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EXAMINER	
CHOW, YUK	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/808,071	FUKUTOKU, SYOUICHI	
	Examiner	Art Unit	
	Yuk C. Chow	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/25/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's arguments filed on 05/25/2007 with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-14, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanbe et al. (US Patent 6,151,016) in view of Yasui et al (US Patent 5,248,963).

As to claim 1, Kanbe discloses a liquid crystal display device (see abstract), being configured such that at least one internal power supply (Fig 13(59)) is automatically changed (see abstract which describes a system switches to auxiliary power supply upon input of a power source OFF signal) from a first power supply (see Fig. 1 (14) to a second power supply (see Fig. 1(10)) different from the first power supply when an input power supply (Fig 13 (71)) fed to the liquid crystal display device is cut off (Fig 13 (60)).

However, Kanbe does not teach internal power supply is a power supply for driving gate lines of a display part in the LCD, is automatically changed using a power supply changeover circuit; a first power supply includes a luminance inclination circuit; a

second power supply includes a power holding circuit; and power supply changeover circuit directly detects the cutoff of the input power supply.

Yasui discloses a circuit for erasing a LCD image comprising a voltage drop detector (Fig. 5(24), which is directly connected to terminal (Fig. 5(21)) and detects power cutoff; a power circuit (Fig. 5(23) which includes a function similar to luminance inclination circuit (see Col. 4 line 40- Col. 5 line 30); and a power holding circuit (Fig. 5(22)).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to implement directly detection of the turning off of the power supply as in Yasui into the LCD device of Kanbe, because the output of the gate bus drive circuit are simultaneously help at the active level by its direct detection, hence results in uniform driving (see Yasui Col. 3 lines 3-22).

For claim 2, combination of Kanbe and Yasui teach:

The liquid crystal display device according to claim 1, wherein a voltage (see Kanbe Fig. 14 (constant voltage output))of said first power supply (see Kanbe Fig. 1 (14)) changes with time (see Kanbe Fig. 16 (source/gate enable signal), and wherein a voltage of said second power supply (see Kanbe Fig. 1 (10)) is attenuated (see Kanbe Col. 13 line 37, auxiliary power source using a capacitor, voltage in capacitor attenuates over time) according to a power outputted as the internal power supply (see Kanbe Fig 13(59), see Col. 8 line 24-31).

For claim 3, combination of Kanbe and Yasui teach:

The liquid crystal display device according to claim 1, wherein a voltage of said first power supply lowers every constant period (see Kanbe Fig. 3,Main Power Source ON Period) and thereafter, returns to an original voltage (see Kanbe Fig 3, Vertical Period ON Level), and wherein a voltage of said second power supply (see Kanbe Fig. 3 Auxiliary Power Source) is kept substantially constant (see Kanbe Fig. 14, Relay Switch Control Signal).

For claim 4, combination of Kanbe and Yasui teach:

The liquid crystal display device according to claim 1, wherein said power holding circuit (see Yasui Fig. 5(22)) configured to hold a power fed by the input power supply (see Kanbe Fig 13 (71)), and wherein said second power supply (see Kanbe Fig. 1(10)) uses the power held in said power holding circuit.

For claim 5, combination of Kanbe and Yasui teach:

The liquid crystal display device according to claim 4, wherein as said second power supply, residual charges (see Kanbe Col. 8 line 27-31) in said power holding circuit (see Kanbe Fig. 13 (59)) are utilized.

For claim 6, combination of Kanbe and Yasui teach:

The liquid crystal display device according to claim 1, wherein said internal power supply is a gate-on power supply (see Kanbe Fig 1 (3)) involved in driving control of the gate signal line (see Kanbe Fig. 2($25_{1,2...m}$)) of the display part.

For claim 7, combination of Kanbe and Yasui teaches:

The liquid crystal display device according to claim 1, wherein, after the input power supply (see Kanbe Fig 13 (71)) is cut off, a voltage based on said second power

supply is outputted to all gate signal lines of the display part (see Kanbe Col 6 line 66-Col.7 line 24, also Col 8 line 1-9).

For claim 8, combination of Kanbe and Yasui teach:

A liquid crystal display device, comprising: a first power supply (see Kanbe Fig. 1 (14)) circuit configured to generate a first power supply from an input power supply (see Kanbe Fig 13 (71)) fed to the liquid crystal display device, wherein said first power supply circuit includes a luminance inclination circuit (see Yasui Fig. 5(23)); a second power supply circuit (see Kanbe Fig. 1 (10)) configured to generate from the input power supply a second power supply different from the first power supply, wherein said second power supply circuit includes a power holding circuit (see Yasui Fig. 5(22)); and a power supply changeover circuit (see Yasui Fig. 5(24)) configured to selectively output, as an internal power supply (see Kanbe Fig 13(59)), one of the first power supply generated in said first power supply circuit and the second power supply generated in said second power supply circuit, wherein said internal power supply is a power supply for driving gate lines of a display part in the liquid crystal display device, and further wherein said power supply changeover circuit directly detects a cut off of the input power supply (see Yasui Col. 4 line 40- Col. 5 line 30).

For claim 9, combination of Kanbe and Yasui teach:

The liquid crystal display device according to claim 8, wherein said power supply changeover circuit (see Yasui Fig. 5(24)) automatically changes (see Kanbe's abstract which describes a system switches to auxiliary power supply upon input of a power source OFF signal) the power supply to be outputted as the internal power supply (see

Kanbe Fig 13(59)) from the first power supply to the second power supply when the input power supply is cut off (see Kanbe Fig 13 (60)).

For claim 10, combination of Kanbe and Yasui teach:

The liquid crystal display device according to claim 8, wherein said power supply changeover circuit (see Yasui Fig. 5(24)) changes the power supply to be outputted as the internal power supply according to a voltage of the input power supply (see Yasui Fig. 5(V1)).

For claim 11, combination of Kanbe and Yasui teach:

The liquid crystal display device according to claim 8, wherein the internal power supply (see Kanbe Fig 13(59)) is a power supply for driving a gate signal line (see Kanbe Fig. $2(25_{1,2..m})$) of a display part (see Kanbe Col 6 line 66 – Col.7 line 24).

For clam 12, combination of Kanbe and Yasui teach:

The liquid crystal display device according to claim 11, wherein said first power supply circuit generates a voltage waveform for reducing luminance unevenness in a direction in which the gate signal line of the display part extends (see Yasui Col. 5 line 51-Col. 6 line 32), and wherein said second power supply circuit generates a voltage waveform whose voltage is constant (see Kanbe Fig. 14, Relay Switch Control Signal).

For claim 13, combination of Kanbe and Yasui teach:

The liquid crystal display device according to claim 8, wherein said first power supply (see Kanbe Fig 1(14)) circuit generates the first power supply whose voltage (See Kanbe Fig 16, Source/Gate Enable Signal) is changed based on an inputted oscillation signal (see Kanbe Fig. 16, Horizontal Synchronizing Signal), and wherein

said second power supply circuit (see Kanbe Fig 1(10)) holds a power by the input power supply (See Kanbe Fig 13(71)) to generate the second power supply (see Kanbe Fig 1(10)).

For claim 14, combination of Kanbe and Yasui teach:

The liquid crystal display device according to claim 8, further comprising a gate driving circuit (see Kanbe Fig.13(53)) configured to be fed with the internal power supply (see Kanbe Fig 13(59)) to drive a gate signal line (see Kanbe Fig 2($25_{1,2...m}$)) of a display part, wherein said gate driving circuit (see Kanbe Fig.13(53)) sequentially outputs signals generated using the first power supply (see Kanbe Fig 1 (14)) to the gate signal lines, and when the input power supply (see Kanbe Fig 13(71)) is cut off, said gate driving circuit outputs a voltage (see Kanbe Fig 15, Gate Driving Signal) of the second power supply (see Kanbe Fig 1(10)) to all the gate signal lines.

For claim 17, combination of Kanbe and Yasui teach:

A liquid crystal display device comprising: a luminance inclination circuit (see Yasui Fig. 5(23)) configured to generate, from an input power supply (see Kanbe Fig. 3(71)) fed to the liquid crystal display device, a voltage waveform for reducing luminance unevenness in a direction in which a gate signal line of a display part extends; a power holding circuit (See Yasui Fig. 5(22)) configured to hold a power by the input power supply; a power supply changeover circuit configured to selectively output one of an output from said luminance inclination circuit and an output from said power holding circuit according to a voltage (See Yasui Fig. 5(V1)) of the input power supply, wherein said power supply changeover circuit directly detects a cut off of the

input power supply (see Yasui Col. 4 line 40- Col. 5 line 30); and a gate driving circuit (See Yasui Fig. 5(17)) configured to be fed with an output of said power supply changeover circuit to drive the gate signal line (see Yasui Fig. 5(G1-Gm)) of the display part.

For claim 18, combination of Kanbe and Yasui teach:

The liquid crystal display device according to claim 17, wherein said power supply changeover (see Yasui Fig. 5(24)) circuit outputs an output from said luminance inclination circuit when a voltage value of the input power supply is higher than a threshold value (see Yasui Fig. 6C(Vth)), and outputs an output from said power holding circuit when the voltage value of the input power supply is equal to or lower than the threshold value (See Yasui Col. 5 lines 31-50).

3. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanbe and Yasui in further view of Lee (US Patent 7,023,511).

As to Claim 15 and 16, Kanbe and Yasui teach the limitation of claim 1 for the reason above.

However, Kanbe and Yasui differ from the claimed invention in that the LCD is not taught to necessarily be a "transflective liquid crystal display device".

Lee teaches a transsflectve liquid crystal display that can be operated as transmissive mode or reflective mode or both at the same time (Col. 4 line 53 – Col. 5 line 11). Lee also indicates the reflective or transflective LCD having a good utilizing

efficiency in power usage (Col. 2 line 64-67), that is an advantage over the conventional LCD device of Kanbe.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use reflective or transflective LCD of Lee's with the LCD device of Kanbe and Yasui, because they both provide greater efficiency in power usage.

4. Claims 19-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanbe and Yasui in further view of Tsuchi et al (US Patent 6,909,414 B2).

As to Claims 19, 20, 21, Kanbe and Yasui teach the limitation of claims 1, 8, 17 respectively above.

However, Kanbe and Yasui does not teach the power supply changeover circuit includes a plurality of resistors and a plurality of transistors.

Tsuchi discloses a driver changeover circuit (see Abstract) using a plurality of resistors (Fig. 9(R0-Rn)) and plurality of transistors (Fig. 10(101-104).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use resistors and transistors for power handling circuit as in Tsuchi into LCD device of Kanbe and Yasui, because it's well known that transistors are efficient (low-lose) device when uses as a power handling switch, especially using a p-channel transistor to connect with low-potential power supply and n-channel transistor to connect with high-potential power supply (See Tsuchi Col. 16 lines 25-59).

As to claims 22, 23 and 24, combination of Kanbe, Yasui and Tsuchi teach the limitation of claims 19, 20 and 21 respectively above.

Tsuchi also teaches plurality of transistors includes two n-channel transistors (Fig. 10(103,104)) and one p-channel (Fig. 10(106)).

As to claims 25, 26 and 27, combination of Kanbe, Yasui teach the limitation of claims 1, 8 and 17 respectively above.

Tsuchi teaches a waveform of an output driving voltage of said first power supply includes an intentionally blunt falling edge (see Fig. 4).

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yuk C. Chow whose telephone number is 571 270-1544. The examiner can normally be reached on 8-6 M-TH E.T..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

YC
08/17/2007

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